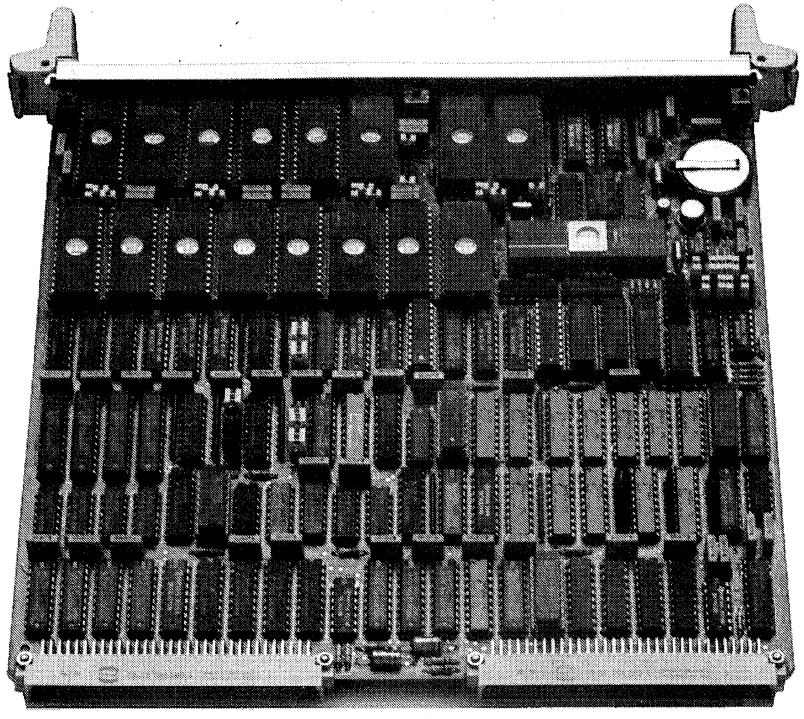
iSBC® MEM/601 MULTIBUS® II UNIVERSAL SITE MEMORY EXPANSION BOARD

- **Supports EPROM, ROM, EEPROM, SRAM, and NVRAM**
- **Sixteen Sites Configured as Two Banks of Eight 28-Pin JEDEC Sockets**
- **Start Addresses for Each Bank Independently Assignable Anywhere on 64K Byte Boundaries Within the 4G Byte iPSB Memory Address Space**
- **Automatic Memory Initialization at Power-Up**
- **Optional On-Board Support for Lithium Battery Backup Memory Protect**
- **MULTIBUS® II Software Interconnect Support for Dynamic Memory Configuration and Diagnostics**
- **Fully Supports Either MULTIBUS II 32-Bit Parallel System Bus (iPSB) or 32-Bit Local Bus Extension (iLBX™ II) Bus**

The iSBC MEM/601 MULTIBUS II Universal Site Memory Board is a member of Intel's line of product offerings that utilize the advanced features of the MULTIBUS II system architecture. The iSBC MULTIBUS II Universal Site Memory Board expands system memory capacity and interfaces across either the MULTIBUS II Parallel System Bus (iPSB) or the high speed Local Bus Extension bus (iLBX II).



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FUNCTIONAL DESCRIPTION

General

The iSBC MEM/601 board contains two banks of eight standard 28-pin 600 mil DIP sockets. Either 28- or 24-pin devices may be inserted on the board. The actual capacity of the board is determined by the type and quantity of components installed by the user. The iSBC MEM/601 board is completely compatible with four different types and densities of devices (see Table 1). In addition, the board can be accessed by either the MULTIBUS II Parallel System Bus (iPSB) or Local Extension Bus (iLBX II).

Memory Array

The sixteen universal memory sites on the iSBC MEM/601 board are partitioned into two banks of 8 sites each. Within each bank the 8 sites are further partitioned into 2 groups of 4 sites each (see Figure 1). Each group of 4 sites can support the device types described in Table 1 and is configurable via an arrangement of push-in jumpers dedicated to each of the four groupings of 4 sites. Devices of the same density and speed must reside within each bank and devices of the same type must reside within each group.

Memory Address Decoding

The memory array is divided into two separate addressable banks. The addressing for each bank is independently software-configurable through MULTIBUS II interconnect space and is on 64K byte boundaries. Software must insure that the address space of one bank does not overlap the address space of the other bank otherwise memory errors would result.

Built-In-Self-Test and Interconnect Subsystem

Self test and diagnostics have been built into the heart of the MULTIBUS II system. These confidence

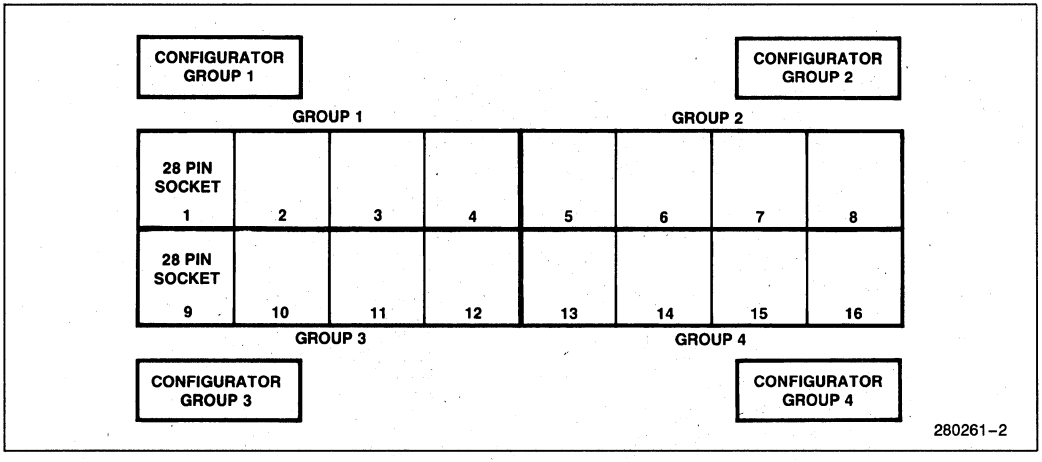

Figure 1. iSBC® MEM/601 Sixteen, 28-Pin Universal Site Memory Array

Table 1. Memory Devices Supported by the iSBC® MEM/601 Board

Type	2K x 8	4K x 8	8K x 8	16K x 8	32K x 8	64K x 8	
EPROM	2716	2732A	2764	27128	27256	27512	
ROM	Yes	Yes	Yes	Yes	Yes	Yes	
EEPROM	2817A	Yes	2864A	Yes	Yes	Yes	+5V Only
SRAM	TC 5516	Yes	TC 5565	Yes	TC 55257	Yes	NMOS and CMOS
Maximum Memory Capacity	32 KB	64 KB	128 KB	256 KB	512 KB	1 MB	

tests and diagnostics improve reliability and reduce manufacturing and maintenance costs. LED 1 (labelled BIST), is used to indicate the status of the built in self test. It is turned on when the BISTs start running and is turned off when the BISTs have successfully executed. Error information from the BISTs is recorded in the interconnect registers accessible to software. The built in self tests are performed by the on-board microcontroller at power-up or on command.

The iSBC MEM/601 board interconnect subsystem consists of an 8751 microcontroller for Built-In-Self-Test (BIST), program storage, status, control registers, and interconnect control logic. The interconnect subsystem receives requests to interconnect space across either the iPSB bus or the iLBX II bus depending on which interface is enabled. The interconnect subsystem is used by the software to configure the hardware.

Battery Backup

The iSBC MEM/601 board supports jumper selectable on-board or off board battery backup operation for CMOS SRAMs. Memory protection for the two memory banks can be supported with +5V from an off board power source or from the optional on board lithium battery. The memory content of the CMOS RAMs is protected during power-up and power-down by the protect signals from the iPSB bus.

Parallel System Bus Interface

The iPSB bus interface supports memory space and interconnect space and provides the capability of 8-, 16-, 24-, and 32-bit transfers,. The iPSB interface can be dynamically activated through the status register of the interconnect space under software control or can be jumper selectable. After a cold reset the iPSB is enabled and the Local Bus Extension (iLBX II) bus is disabled.

Local Bus Extension Interface

The iSBC MEM/601 board provides 8-, 16-, 24-, and 32-bit transfers across the Local Bus Extension (iLBX II) interface. The iLBX II bus interface is enabled by the status register of the interconnect space and can therefore be dynamically changed through software. It is also jumper selectable. After a cold reset, the iLBX II interface is disabled. The iPSB bus interface is always disabled when the iLBX II bus is enabled.

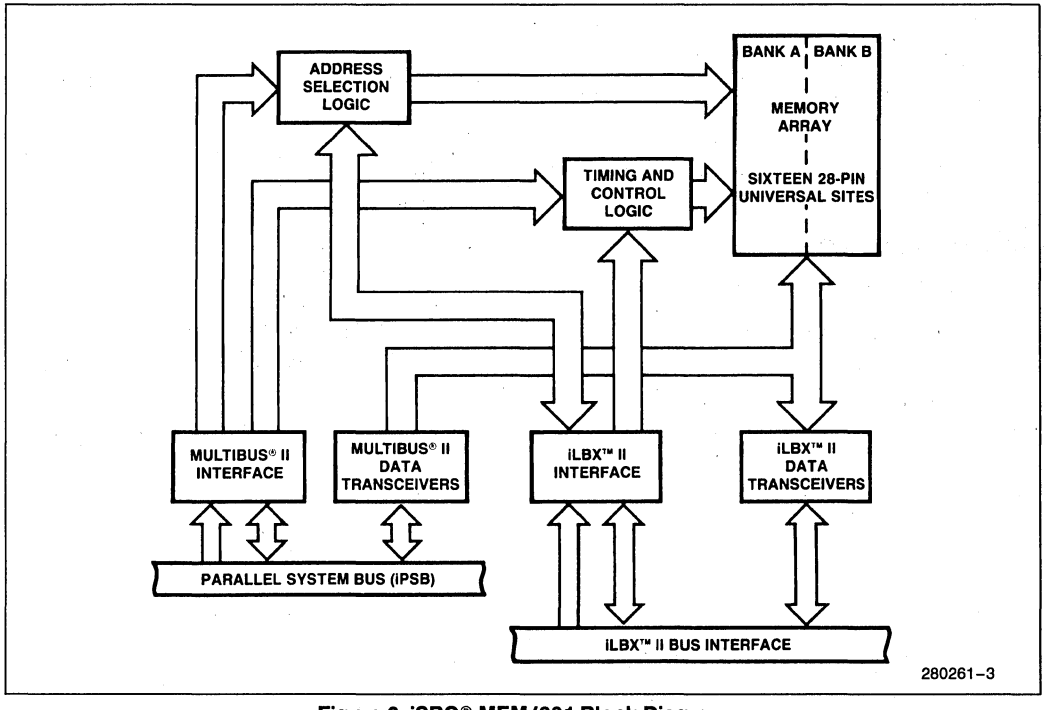

Figure 2. iSBC® MEM/601 Block Diagram

SPECIFICATIONS

Word Size 8-, 16-, 24, and 32-bits

Memory Size

Sockets are provided for up to sixteen JEDEC compatible 28-pin devices which can provide up to 1.0M Byte of EPROM/ROM/SRAM memory.

Access Times

	iPSB Bus	iLBX™ II Bus*
Read Cycle Without Replier Busy	300 ns	250 ns
Write Cycle Without Replier Busy	300 ns	250 ns
Read/Write with Agent Error	100 ns	10 ms

NOTES:
Access times are calculated without device speed included. True access times across either bus must include device access time and must be in 100 ns increments for the iPSB bus. Above calculations assume 1 bus cycle. Refer to the iSBC MEM/601 Memory Board User's Guide for exact formula to determine access times for specific operating configurations.

*Access times across the iLBX II bus assumes an 8.0 MHz bus clock. The actual formula is as follows:

T = 2(C) + D where: T is iLBXII Bus access time
C is 1/f, f = iLBX II Bus clock speed
D is Device access time

Power Requirements

Current with 2764A EPROMS installed @ +5V: 4.5A

Current with 2864A EEPROMS installed @ +5V: 5.5A

At 3V and 300 mA hours lithium battery rating, the expected retention time for standard CMOS SRAM memories will be approximately 24–36 hours.

ENVIRONMENTAL REQUIREMENTS

Temperature: Inlet air at 200 LFM airflow over boards

Non-operating: −40 to 70°C

Operating: 0 to 55°C

Humidity:

Non-operating: 95% RH @ 55°C
Operating: 90% RH @ 55°C

Physical Dimensions

The iSBC MEM/601 board meets all MULTIBUS II mechanical specifications as presented in the MULTIBUS II specification (#146077).

Double High Eurocard Form Factor

Depth: 220 mm (8.6 in.)
Height: 233 mm (9.2 in.)
Front Panel Width: 20 mm (0.784 in.)
Weight as shipped from factory: 543g (19 oz.)

Reference Manuals

#149149—iSBC MEM/601 Memory Board User's Guide

#146077—Intel MULTIBUS II Bus Architecture Specification

Manuals may be ordered from any Intel Sales Representative, Distributor Office, or from the Intel Literature Department, 3065 Bowers Ave., Santa Clara, CA., 95051.

Ordering Information

Part Number	Description
SBCMEM601	MULTIBUS II Universal Site Memory Expansion Board